REMARKS

The Official Action mailed August 26, 2002 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to December 26, 2002. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicants note with appreciation the consideration of the Information Disclosure Statements filed on June 14, 2000 and July 21, 2000. However, Applicants have not yet received acknowledgment of the Information Disclosure Statement filed on November 13, 2001. Applicants respectfully request that the Examiner provide an initialed copy of the Form PTO-1449 with the following Official Action evidencing consideration of this Information Disclosure Statement.

Claims 1-52 are pending in the present application, of which claims 1, 8, 15, 23, 31, 36, 42 and 48 are independent. Claims 1, 3, 8, 10, 15, 17, 23, 25, 31, 33, 36, 38, 42, 44, 48 and 50 have been amended herewith. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

The claims of the present application recite a TFT structure shown in Figure 2F and described in Example 4 of the specification. All of the independent claims have been amended herewith so as to include a feature of a first inorganic insulating film as supported by reference numeral 214 in Figure 2F and on page 22, line 1 of the specification. All independent claims now recite a combination of a first inorganic insulating film and a second insulating film comprising an organic resin over the first inorganic insulating film.

The Official Action rejects claims 1-4, 6-11, 13-18, 20-26, 28-30 and 48-51 as obvious based on U.S. Patent 5,153,142 to Hsieh and U.S. Patent 5,273,910 to Tran et al. As stated in MPEP § 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed

invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The Official Action contends that it would have been obvious to one of ordinary skill in the art to coat the first insulating film (20) in Hsieh's device with a polyimide layer as taught by Tran in order to obtain a smooth planarization layer. Applicant respectfully disagrees and asserts that the Official Action has failed to establish a *prima facie* case of obviousness.

As the Examiner admits, Hsieh fails to disclose or suggest the second insulating film comprising an organic resin. Tran teaches in column 9, lines 58-61 that the planarization layer 53 is formed from an insulating material such as SiO_x, SiN_x, silicon oxide nitride, or combination thereof, and the planarization may be formed from a polyimide. Although Tran may teach a combination of the insulating films 53a-53e (col. 9, line 66-col. 10, line 8) and as shown in Figs. 5a and 5b for the planarization, it appears that Tran fails to disclose the combination of the first inorganic insulating film and the second insulating film comprising an organic resin.

It is respectfully submitted that the combination of these references and the above assertions in the Official Action are based on improper hindsight because neither Hsieh nor Tran discloses or suggests the combination of a first inorganic insulating film and a second insulating film comprising an organic resin, and further because even Tran itself fails to teach the combination of the first inorganic insulating film and the second insulating film comprising an organic resin as mentioned above.

In addition, it is respectfully submitted that the Official Action has failed to provide a sufficient basis that one of skill in the art would have been motivated to combine the reference teachings to achieve the present invention. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness. The mere fact that references can be combined or modified does not render the resultant combination

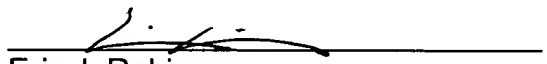
obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). See MPEP 2143.01. In the present combination, there is no disclosure or suggestion that one of skill in the art would have recognized Hsieh's device to have an uneven surface or that the planarization layer of Tran should be included in the device. Absent some suggestion that the references should be combined, it is respectfully submitted that an insufficient motivation has been demonstrated and that a *prima facie* case of obviousness cannot be maintained.

Moreover, the claimed invention recites that the second insulating film comprising resin is formed over the first inorganic insulating film. Applicants believe that this feature cannot be obtained even when these references are combined. Therefore, since the references, whether taken alone or in combination, fail to disclose or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained for this further reason. Favorable reconsideration is requested.

The Official Action next rejects claims 5, 12, 17, 19, 31-47 and 52 as obvious based on the combination of Hsieh, Tran and U.S. Patent 5,027,185 to Liauh. It is respectfully submitted that Liauh does nothing to overcome the deficiencies noted above with respect to Hsieh and Tran and that the rejection of these claims is improper for the same reasons as discussed above. Favorable reconsideration is requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 1, 3, 8, 10, 15, 17, 23, 25, 31, 33, 36, 38, 42, 44, 48 and 50 as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed [on] over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed over said second insulating film.

3. (Amended) A semiconductor device of claim 1 wherein said first inorganic insulating film comprises silicon oxide.

8. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed [on] over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a pixel electrode formed over said second insulating film.

10. (Amended) A semiconductor device of claim 8 wherein said first inorganic insulating film comprises silicon oxide.

15. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed [on] over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed over said second insulating film.

17. (Amended) A semiconductor device of claim 15 wherein said first inorganic insulating film comprises silicon oxide.

23. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed [on] over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions; and

a transparent pixel electrode formed over said second insulating film.

25. (Amended) A semiconductor device of claim 23 wherein said first inorganic insulating film comprises silicon oxide.

31. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed [on] over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions, wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions.

33. (Amended) A semiconductor device of claim 31 wherein said first inorganic insulating film comprises silicon oxide.

36. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed [on] over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions, wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions.

38. (Amended) A semiconductor device of claim 36 wherein said first inorganic insulating film comprises silicon oxide.

42. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed [on] over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions, wherein said electrode has a laminate structure including a first conductive film comprising aluminum and a second conductive film comprising a different material from said first conductive film;

a transparent pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions, wherein said electrode comprises a same material as said conductive layer.

44. (Amended) A semiconductor device of claim 42 wherein said first inorganic insulating film comprises silicon oxide.

48. (Amended) A semiconductor device comprising:

a semiconductor layer having at least first and second impurity regions and a channel region formed on an insulating surface;

a gate insulating film adjacent to said semiconductor layer;

a gate electrode adjacent to said gate insulating film;

a first inorganic insulating film covering at least said gate electrode and said semiconductor layer except for contact holes opened therein;

a second insulating film comprising an organic resin formed [on] over said first inorganic insulating film;

an electrode formed over said second insulating film and connected to one of said first and second impurity regions;

a pixel electrode formed over said second insulating film and electrically connected to said one of said first and second impurity regions through said electrode; and

a conductive layer formed over said second insulating film and connected to the other one of said first and second impurity regions,

wherein a portion of said pixel electrode is located below said electrode.

50. (Amended) A semiconductor device of claim 48 wherein said first inorganic insulating film comprises silicon oxide.